# SYSTEM AND METHOD TO SCREEN DEFECT RELATED RELIABILITY FAILURES IN CMOS SRAMS

## ABSTRACT

A method for testing a semiconductor wafer. An array of probes is coupled to the semiconductor wafer. Then a voltage difference is applied across a plurality of adjacent metal line pairs (e.g., wordline and/or bitline pairs) of one or more SRAM arrays of at least one die. Application of the voltage difference induces failure of metal stringers or defects between the adjacent lines. Additionally, the voltage can be applied across respective pairs of substantially all parallel metal lines of the one or more SRAM arrays of more that one die of the semiconductor wafer.

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